

NSLS2 Injector Timing

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Contents

| | | |
|----------|--|----------|
| 1 | Overview | 2 |
| 2 | Requirements | 2 |
| 2.1 | Process Variables | 2 |
| 3 | Cycle Definition | 2 |
| 4 | Event Codes | 3 |
| 4.1 | Linac+Booster 1 Hz cycle | 6 |
| 4.2 | Linac+Booster 2 Hz cycle | 6 |
| 4.3 | Linac+Booster stacking cycle | 6 |
| 4.4 | Booster PSC Update Event (#27) | 6 |
| 5 | Storage Ring Filling | 6 |
| 6 | Device Timing | 7 |
| 6.1 | Booster Kicker Magnets | 7 |
| 7 | Process Variables | 9 |
| 8 | User Interface | 9 |

1 Overview

This document describes the proposed machine timing configuration and user controls for Booster commissioning.

2 Requirements

1. Support independant operation of Linac for testing at 1, 2, 5, and 10Hz.
2. Support independant testing of Booster timing.
3. Support Booster operating modes: 1Hz, 2Hz, and stacking.

2.1 Process Variables

The following are the minimum set of PVs which would be provided.

1. Provide a single timestamp for each booster cycle which can be used to simplify later retrieval.
2. Provide the timestamp of the previous cycle for diagnostics with long readout latency.
3. Provide the number of PSC clock ticks in the 1Hz and 2Hz cycle periods.
4. Allow operators to select Linac timing modes. This will consist of several individual controls
 - (a) Select Linac Mode: Off, 1Hz, stacking, 2Hz, 5Hz, or 10Hz.
 - (b) Select Booster Mode: Off, 1Hz, stacking, or 2Hz.
 - (c) Load selected modes.
5. Provide status:
 - (a) Currently running modes for Linac and Booster
 - (b) Current modes compatible with injection of beam into booster.
 - (c) If selected next modes can be loaded (based on current machine state).
 - (d) Timing operation status (running, stopped).
 - (e) Cycle counter.

3 Cycle Definition

For the purposes of configuration an injector cycle is viewed on a 1 second scale (see figure 2). Here 1 second is defined as as 127281000 ticks of the Timing System clock or equivalently 509124000 ticks of the ~500 MHz RF reference clock. This is broken down into two 500 ms periods (63640500 timing ticks) and further into 10 periods of 100 ms (12728100 timing ticks).

In real (wall clock) time duration of the 1 second cycle is 1.018900096 seconds. This assumes an RF clock frequency of exactly 499.68 MHz.

These numbers are selected to satisfy the constraints imposed by the necessity that the cycle periods should be multiples of the clocks shown in figure 1. The divider N gives the ~10Hz period. The constraints placed on N can be expressed as:

$$\begin{aligned}
N &= 6 \cdot M \\
N &= \frac{14}{3} \cdot P \\
N &= 12540 \cdot Q \\
N &= \frac{25}{2} \cdot R \\
N &= \frac{5}{2} \cdot S
\end{aligned}$$

Given that M (LN 500MHz LLRF), N (Timing System), P (LN 3GHz LLRF), Q (Orbit feedback and ring revolution clocks), R (BR LLRF), and S (BR LLRF) must be integers, it can be seen that the first divider N which produces a frequency $\leq 10Hz$ is $N = 12728100$. The others parameters are then $M = 2121350$, $P = 2727450$, $Q = 1015$, $R = 1018248$, $S = 5091240$.

The number of 10 KHz PSC (Power Supply Controller) clock ticks during each 1 Hz cycle is thus 10150.

4 Event Codes

The event codes allocated for use in the injector are:

| Event # | Function |
|---------|---------------------------------|
| 15 | Linac pre-trigger |
| 16 | Linac e^- source trigger |
| 21 | BR Injection #1 (all modes) |
| 22 | BR Injection #2 (stacking mode) |
| 23 | BR Charge IS kickers |
| 25 | Booster T0 |
| 26 | Booster Extract |
| 27 | Booster PSC Sync |
| 28 | BR Charge XS kickers |

Notation:

N_X Number of ticks in $\frac{X}{1000}$ of the total cycle length. N_{1000} is equal to $10 \cdot N$ as derived in section 3.

R_X Number of ticks in X ms (wall clock) assuming an RF reference clock frequency of exactly 499.68 MHz.
($R_X = 124920 \cdot X$)

T_M Period of machine M ($BR = 66$ or $SR = 330$)

L_Y Time of previous occurrence of event Y in this sequence.

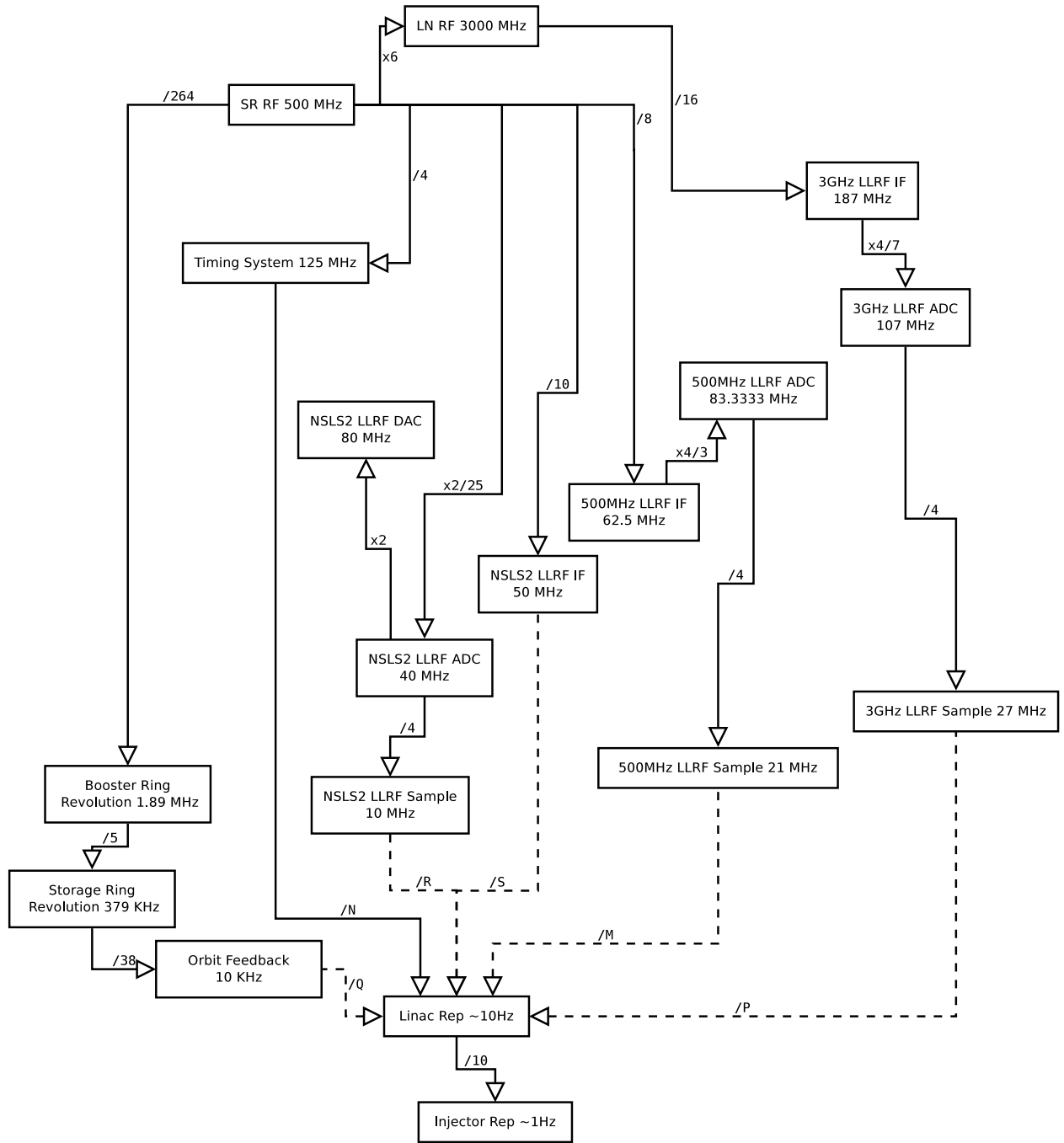


Figure 1: Constraints on the selection of the 10 Hz period

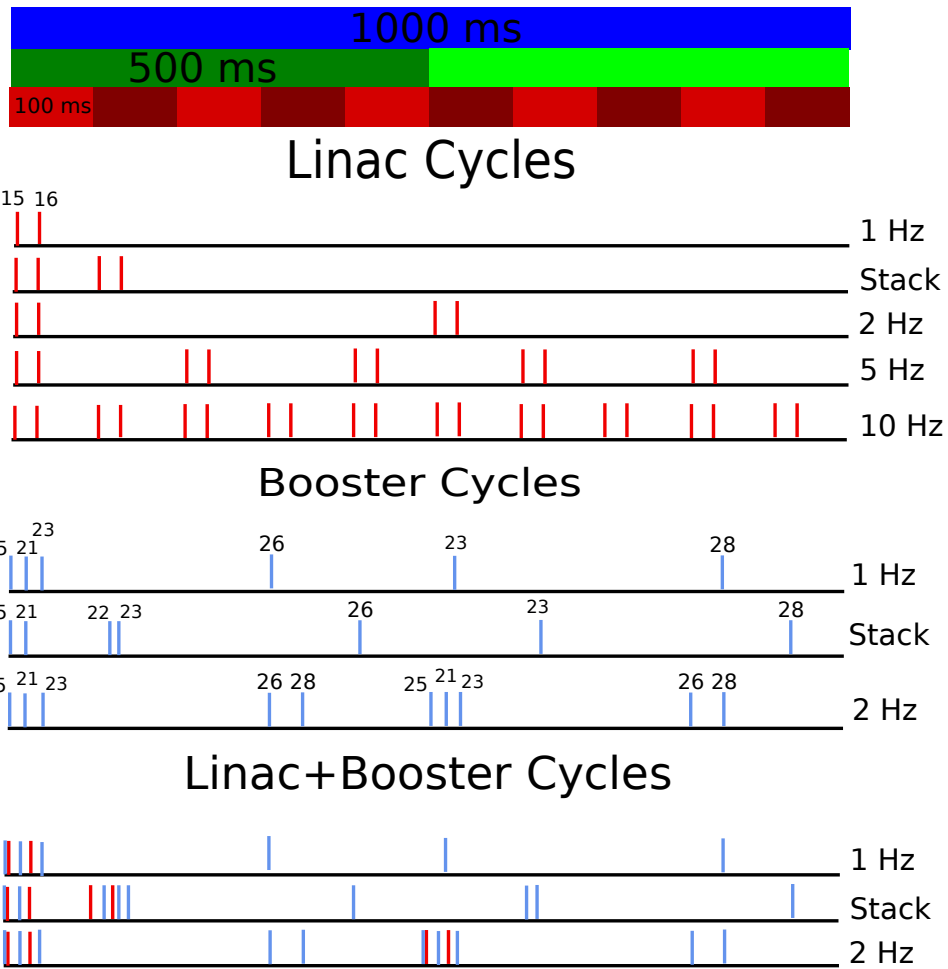


Figure 2: Order and approximate time of injector events

4.1 Linac+Booster 1 Hz cycle

| Event # | Delay Calc | Delay Ticks | EGU | Function |
|---------|----------------------------|-------------|--------|---|
| 25 | Reference | 0 | 0 ns | Starts PSCs and device cycle start time |
| 15 | $L_{25} + 1$ | 1 | 8 ns | Start Linac Cycle start |
| 21 | $L_{25} + 303 * T_{SR}$ | 999900 | 8 ms | Booster injection #1 |
| 16 | $L_{15} + R_{10}$ | 1249201 | 10 ms | Linac Electron source trigger |
| 23 | $L_{21} + R_4$ | 1499580 | 12 ms | BR Charge IS kickers |
| 26 | $L_{25} + T_{SR} * 113600$ | 37488000 | 300 ms | Booster Extraction |
| 23 | $L_{23} + N_{500}$ | 65140080 | 521 ms | BR Charge IS kickers |
| 28 | $L_{26} + N_{500}$ | 101128500 | 809 ms | Booster XS Kicker Charge |

4.2 Linac+Booster 2 Hz cycle

| Event # | Delay Calc | Delay Ticks | EGU | Function |
|---------|----------------------------|-------------|--------|---|
| 25 | Reference | 0 | 0 ns | Starts PSCs and device cycle start time |
| 15 | $L_{25} + 1$ | 1 | 8 ns | Start Linac Cycle start |
| 21 | $L_{25} + 303 * T_{SR}$ | 999900 | 8 ms | Booster injection #1 |
| 16 | $L_{15} + R_{10}$ | 1249201 | 10 ms | Linac Electron source trigger |
| 23 | $L_{21} + R_4$ | 1499580 | 12 ms | BR Charge IS kickers |
| 26 | $L_{25} + T_{SR} * 113600$ | 37488000 | 300 ms | Booster Extraction |
| 28 | $L_{26} + R_4$ | 37987680 | 304 ms | Booster XS Kicker Charge |

4.3 Linac+Booster stacking cycle

| Event # | Delay Calc | Delay Ticks | EGU | Function |
|---------|----------------------------|-------------|--------|---|
| 25 | Reference | 0 | 0 ns | Starts PSCs and device cycle start time |
| 15 | $L_{25} + 1$ | 1 | 8 ns | Start Linac Cycle start |
| 21 | $L_{25} + 303 * T_{SR}$ | 999900 | 8 ms | Booster injection #1. |
| 16 | $L_{15} + R_{10}$ | 1249201 | 10 ms | Linac Electron source trigger |
| 15 | $L_{15} + N_{100}$ | 12728101 | 102 ms | 2nd Linac Cycle start |
| 22 | $L_{21} + N_{100}$ | 13728000 | 110 ms | Booster injection #2 |
| 16 | $L_{16} + N_{100}$ | 13977301 | 112 ms | 2nd Linac Electron source trigger |
| 23 | $L_{22} + R_4$ | 14227680 | 114 ms | BR Charge IS kickers |
| 26 | $L_{25} + T_{SR} * 151418$ | 49967940 | 400 ms | Booster Extraction |
| 23 | $L_{23} + N_{500}$ | 77868180 | 623 ms | BR Charge IS kickers |
| 28 | $L_{26} + N_{500}$ | 113608440 | 909 ms | Booster Extraction Kicker Charge |

4.4 Booster PSC Update Event (#27)

This is a special software (asynchronous) event to signals all Booster PSCs to switch their ramp tables at the next start trigger. This event may not be sent for every cycle.

5 Storage Ring Filling

The function of the injector is place electrons in the storage ring. During booster extraction, the first electron bunch to leave to booster will be placed into one of the 1320 RF buckets of the storage ring. A control which

| Device | Function | Res. (ns) |
|-----------------------|--------------------------|-----------|
| cPCI-EVRTG-300 | Electron source trigger | 1 |
| Cryoelectra DRFM 500 | Linac prebuncher LLRF | 48.0 |
| Cryoelectra DRFM 3000 | Linac other LLRF | 37.0 |
| Acqiris ADC | ICT measurement | 8.0 |
| BINP ADC200 | ? | ? |
| BINP VSDC | Power supply diagnostics | ? |
| Prosilica GigE camera | Visual beam diagnostics | 8.0 |
| PSC | Ramping power supplies | 100320.0 |
| BNL CFC | Booster LLRF | 100.0 |
| BNL BPM | Transverse beam position | 2640.0 |
| BINP Kicker | Pulsed magnets | 0.4 |
| BNL Kicker | Pulsed magnets | 0.4 |

Table 1: Effective trigger resolution of devices in the injector

allows operator selection of this SR RF bucket is required. The range for this control is then up to one SR period (2.64 us).

Due to the fact that this control must provide single bucket (2 ns) resolution, this control can not be implemented solely by changing the event delays in the EVG. Some change must be made to the EVR delay channels with better resolution.

To implement this selection control it will be necessary to change some event times and channel delays. To maintain calibrations, it is desirable that the relative delays of certain channels remain the same. There are two difficulties with this.

1. The relation between a regular channel with 8ns resolution and a special channel (CML/GTX) with ≤ 2 ns resolution can not be maintained.
2. Some devices sample the trigger pulse received from the EVR with a clock < 125 MHz. This gives an effective trigger resolution > 8 ns.

Table 1 lists triggered devices in the injector and gives effective trigger resolution (limited by device or EVR). This includes some devices which are not sensitive to start time (eg. integrating).

One possible implementation for targeting some bucket B is to apply a course delay $C = B/4$ to all injector timing events. An additional fine delay would be calculated from $F = B\%4$. The fine delay would be applied to the electron source trigger and other device with a trigger resolution < 8 ns.

6 Device Timing

6.1 Booster Kicker Magnets

The Booster kicker magnet power supplies expect two electrical trigger inputs. One trigger begins the charging process, the second triggers a discharge. The timing for these signals in the CW operating modes is shown in figure 3. The PSC start trigger is also shown for reference.

The start discharge triggers for IS kickers 1 and 2 are mapped to event 22 only. IS kickers 3 and 4 are mapped to both events 21 and 22. The XS kickers are mapped only to event 26.

Booster Kicker Triggers

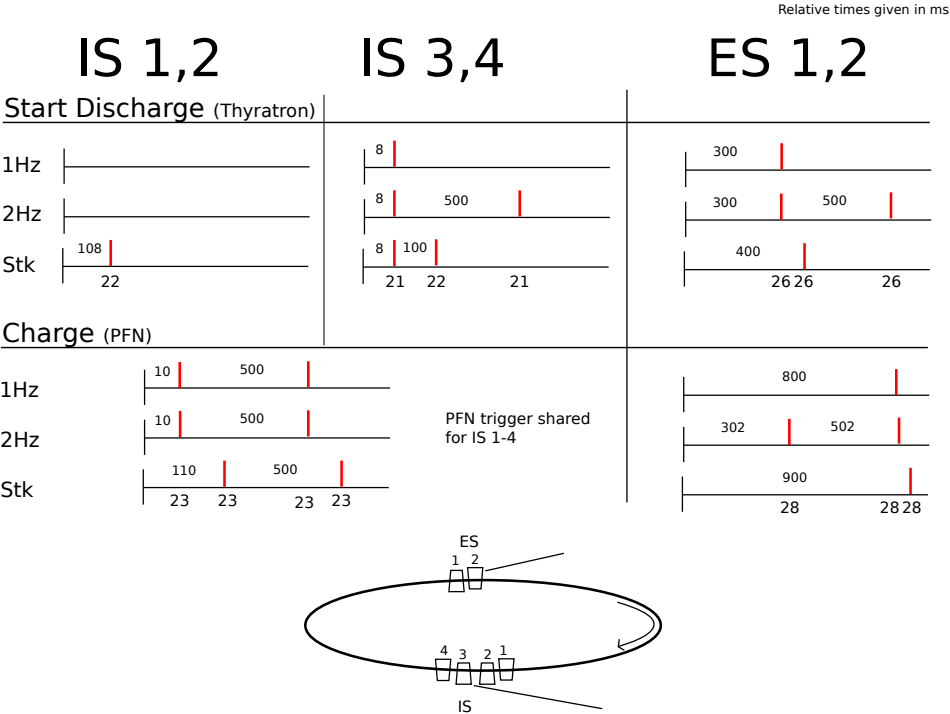


Figure 3: Electrical trigger signals for kicker PS types in each Booster mode

The charge triggers for each kicker group is given a special event due to the unique requirements of these devices.

The IS kickers will be charging at all times during operation. It is desirable that the charging power supplies be started just after a discharge.

For power supplies used for the kickers will stop charging at a fixed 500 ms after a charging trigger is received. Thus for the IS kickers a second charging trigger is needed 500 ms after the first.

The XS kickers should begin charging 500 ms before the next discharge.

An example configuration for the Event Receiver (EVR) channels would be

| Name | Event(s) | Delay from Event | Pulse Width |
|------------------------|----------|------------------|-------------|
| IS 3,4 Start Discharge | 21,22 | 2 ms | 20 us |
| IS 3,4 Charge | 23 | 0 ms | 20 us |
| IS 1,2 Start Discharge | 22 | 2 ms | 20 us |
| IS 1,2 Charge | 23 | 0 ms | 20 us |
| XS Start Discharge | 26 | 2 ms | 20 us |
| XS Charge | 28 | 0 ms | 20 us |

7 Process Variables

In order to satisfy the requirements stated in section 1 the following PVs are provided.

All injector EVRs will be loaded with local counter PVs to provide Booster and Linac timestamps with minimum delivery latency.

- \$(SYS)-TS{EVR:\$(EVR)}Cnt:BR-I
- \$(SYS)-TS{EVR:\$(EVR)}Cnt:BRPrev-I

The relation between the ~10 KHz orbit feedback clock period (used for all PSCs) and the injector repetition clock periods are given available. The values of the first two PVs will remain unchanged unless the timing config is updated. The third will change to reflect the current Booster timing mode.

- BR-TS{}Ratio:10Kto1-I
- BR-TS{}Ratio:10Kto2-I
- BR-TS{}Ratio:10K-I

8 User Interface

The current operator (figure 4) and expert (figure 5) control panels.

The operator panel shows the current timing modes in the right pane. The left pane allows a new timing configuration to be prepared and applied in two separate steps. To do this a user selects from the possible modes for the Linac and Booster. The 'Apply' button will write the new configuration to the Event Generator.

The 'Sequence commit requires' selection allows the operator to place restrictions on the selectable modes. Currently selections are 'Allow any' and 'Require BR Inject'. The second allows only modes which are compatible with injection from Linac to Booster. If an invalid selection is made then clicking the 'Apply' button has no effect.

The expert display contains some diagnostic information and two bit masks which can be used to prevent certain modes from being selected.

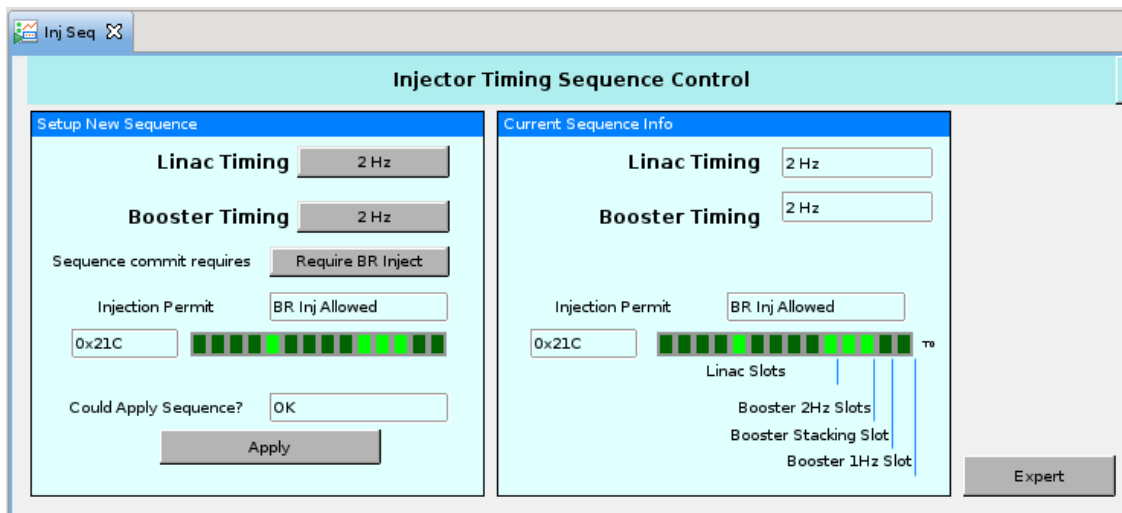


Figure 4: Operator Injector Timing Panel

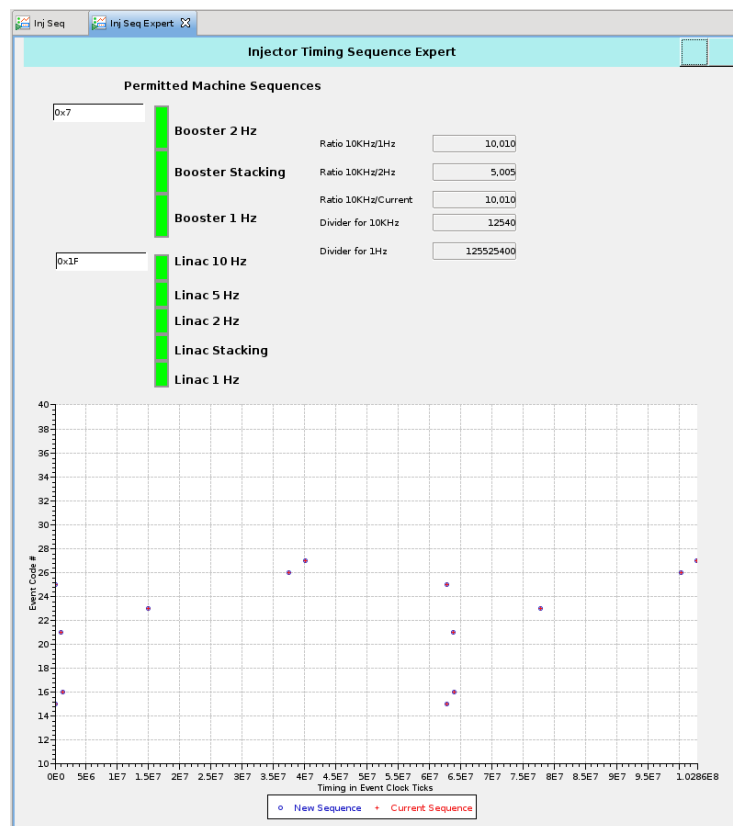


Figure 5: Expert Injector timing display